

ESDLC3V3OD

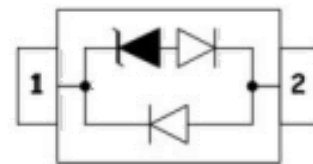
Description

ESDLC3V3OD is designed to protect voltage sensitive components from ESD and transient voltage events. Excellent clamping capability, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its small size, ultra-low capacitance values , it is very suitable for signal port and board space speed transmission is very small places, such as Ethernet, mobile phones , MP3 players, digital cameras and other portable.

Features

- ◆ Operating voltage: 3.3V
- ◆ Ultra low leakage: nA level
- ◆ Package: SOD-323
- ◆ Protects one I/O line (unidirection)
- ◆ Low clamping voltage
- ◆ Complies with following standards:
 - IEC61000-4-2 (ESD) immunity test
 - Air discharge: $\pm 15\text{KV}$
 - Contact discharge: $\pm 8\text{KV}$
 - IEC61000-4-4 (EFT): 40A (5/50ns)
 - IEC61000-4-5 (Lightning): 12A (8/20 μs)

SOD-323



Applications

- ◆ Cell Phone Handsets and Accessories
- ◆ Microprocessor based equipment
- ◆ Personal Digital Assistants (PDA's)
- ◆ Notebooks,Desktops,and Servers
- ◆ Portable Instrumentation
- ◆ Peripherals
- ◆ USB Interface

Absolute Maximum Ratings ($T_a=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
IEC 61000-4-2 ESD Voltage (Air Model)	V_{ESD}	± 15	KV
IEC 61000-4-2 ESD Voltage (Contact Model)		± 8	
Peak Pulse Power(8/20us)	P_{PP}	350	W
Lead Solder Temperature – Maximum (10 Second Duration)	T_{L}	260(10 sec)	$^{\circ}\text{C}$
Operating Temperature Range	T_{J}	-55~ +150	$^{\circ}\text{C}$
Storage Temperature Range	T_{STJ}	-55~ +150	$^{\circ}\text{C}$

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Electrical Characteristics (Ta=25°C unless otherwise specified)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Reverse stand-off voltage	V_{RWM}				3.3	V
Breakdown voltage	V_{BR}	$I_T=1mA$	4			V
Reverse leakage current	I_R	$V_R=V_{RWM}$			40	μA
Clamping voltage	V_C	$I_{PP}=1A, t_p=8/20\mu s$			5.15	V
		$I_{PP}=8A, t_p=8/20\mu s$			13.9	V
Junction capacitance	C_J	$V_R=0V, f=1MHz$			0.4	pF

Characteristics Curves

Figure 1- Power Derating Curve

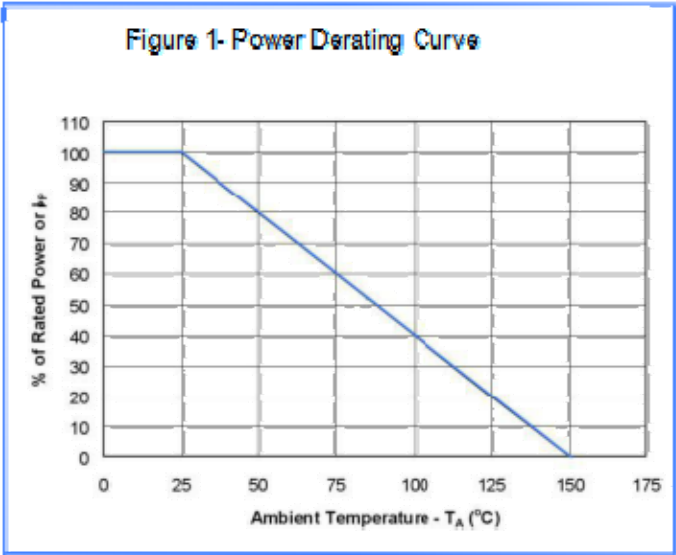


Figure 2- ESD Pulse Waveform (according to IEC 61000-4-2)

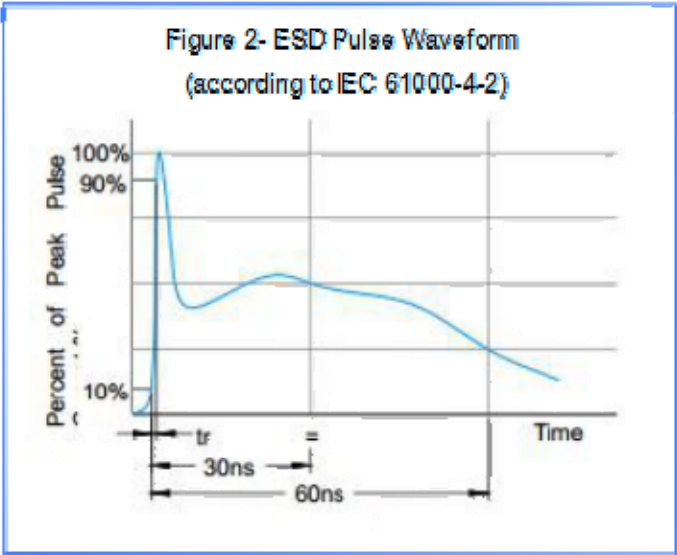
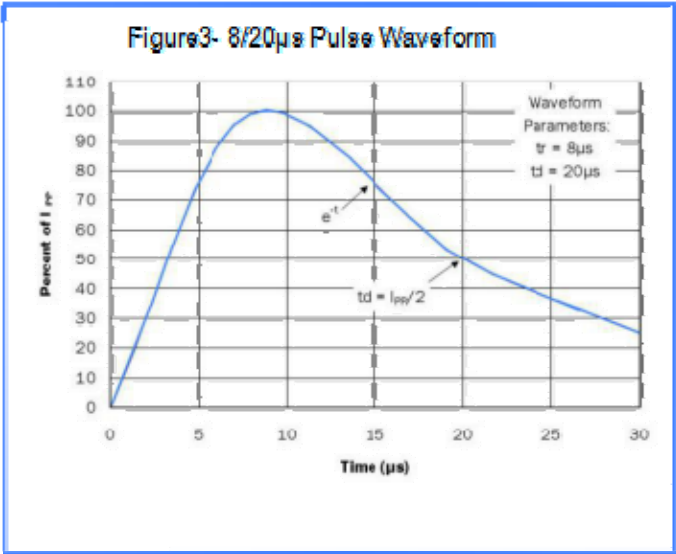


Figure3- 8/20µs Pulse Waveform



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Package Outline

SOD-323

